COMPENSATING DIFFERENCES BETWEEN MEASUREMENT AND CALIBRATION WAFER IN PROBE-TIP CALIBRATIONS

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Abstract — **Differences in probe-tip-to-line geometry and substrate permittivity between measurement and calibration wafer deteriorate measurement accuracy. In this paper, we compare the accuracy of several models for the probe-to-line transition based on measurements as well as 3-D simulations of various GaAs CPW lines. This shows that 3-D simulations may be used to determine the parasitics at the probe tip as an alternative to measurement based methods. In general, models using 4 error-parameters are preferred to the Y_p- or TL-based model as they provide a higher accuracy while the same amount of measurements is required to implement them.**

I. INTRODUCTION

Precise measurements at the component level are essential to obtain designs operating within their target specifications. An accurate "on-wafer" fabrication of calibration standards is difficult with non-precision processing techniques. Many practical measurements therefore rely on an "off-wafer" calibration using a calibration substrate of an external manufacturer. Usually both contact geometry and substrate differ between the calibration structures and the device under test (DUT). A technique is thus needed to account for these differences as they deteriorate the measurement accuracy [1, 2]. The probe-tip discontinuities also have a large effect on the extracted characteristic impedance of the measured lines [3-5] no matter whether an on- or off-wafer calibration is being used as the width and slot of the measured lines usually differs from the calibration structures. Techniques are hence needed to accurately compensate for the probe tip discontinuities.

Previously, we reported in [1, 5] 2 techniques which characterise the discontinuities near the probe-tip based on the measurements of two lines with different length. This paper verifies the performance of several characterisation techniques for the first time using 3-D simulations of the probe-tip-to-line connection. This is performed for various GaAs CPW lines. This will show that 3-D simulations may be used to determine the probe-tip parasitics. 3-D simulations are further used to investigate the accuracy of the methods.

The models compared in this work are briefly described in section II. In section III, the accuracy of the techniques is compared for the deembedding of various GaAs CPW lines.

II. PROBE-TIP DISCONTINUITY MODELS

The measured lines usually do not have the same contact geometry as the calibration standards and also the substrate may differ (Figure 1). This leads to a different behaviour of the shunt-stub underneath the probe-tip and a step-in-width between probe and strip. The location of the probe-tips is also not known exactly. The methods should hence be able to accurately compensate for a shunt admittance at the probe-tip, some extra inductance due to the step-in-width and a reference plane transformation due to the not precisely known location of the probe-tips. In this work, we assume that the S-parameters, representing the probe-tip to line transition have been obtained, e.g., using the technique described in [5].

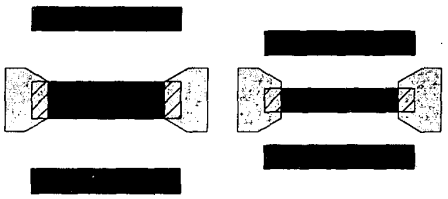

Figure 1: Differences between calibration wafer (left) and measurement wafer (right): different substrate and contact-geometry.

A. Y_pZ_s-model: Arbitrary Series Impedance and Shunt Admittance

The Y_pZ_s-model (Figure 2 (a)), proposed in [1], can determine an arbitrary series impedance (Z_s) and shunt admittance (Y_p) at the probe-tip. The impedances Z_s and Y_p can take any arbitrary form but for simplicity, Z_s can be regarded as a series inductance (L_S) and resistance (R_S), while Y_p can be regarded as a parallel conductance (G_g) and capacitance (C_g). It is therefore mainly a lumped model of a short transmission line. Losses due to a

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different contact geometry are represented by R_S and G_g, differences in contact geometry and substrate permittivity by L_S and C_g (e.g. the difference in open-end effect of the shunt stub underneath the probe-tip or the step-in-width between probe-tip and strip). Small errors in the probe position are accounted for by C_g and L_S.

The transformer (Figure 2) appears due to the characterisation technique used for the determination of the error-boxes (measurement of 2 lines with different length).

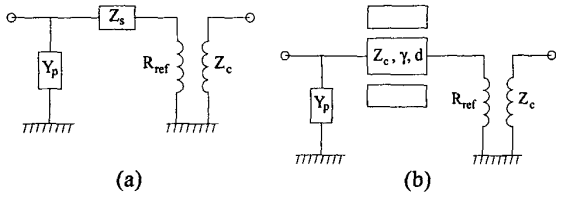

Figure 2: (a) Y_pZ_s-model: the model can account for an arbitrarily large shunt (Y_p) and series (Z_S) impedance. (b) Y_pTL-model: the model can account for an arbitrarily large shunt admittance (Y_p) and reference plane transition (distance d).

B. Y_pTL-model: Arbitrary Reference Plane Transformation and Shunt Admittance

The Y_pTL-model (Figure 2 (b)), proposed in [5], is insensitive to an arbitrary shunt admittance (Y_p) at the probe tips and to an arbitrary shift in the location of the reference plane.

C. Symmetric Y- and Z-matrix based Models

A Y- or Z-matrix based model may also be used to represent the error-boxes (Figure 3). These models consist of a Y or Z-parameter representation of a short transmission line section and assume a symmetric error-box model (note, however, that the physical layout of the discontinuity is asymmetric). The values of the errorbox elements may be obtained in a similar way as outlined in [5] for the Y_pZ_s- and Y_pTL-model.

The models cannot account for an arbitrarily large reference plane transition, however, for practical cases, satisfactory results may be obtained.

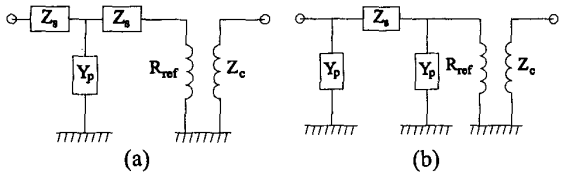

Figure 3: Y-based (a) and Z-based (b) models: a symmetric errorbox is assumed.

D. Single Y_p and TL-models

The TL-model and Y_p model proposed respectively in [3] and [2, 4] only account for an arbitrary reference plane transition or an arbitrary shunt admittance at the probe tip.

III. Evaluation of the Accuracy of the Methods

A. Measurement Set-up

Measurements have been performed using Cascade wafer probes (pitch 100 μm) and an HP8510 network analyzer. The system was calibrated with TRL, using the LRM ISS G-S-G Alumina substrate (ε_r=9.9) of Cascade Microtech (strip=50 μm, slot=25 μm). The reference plane was set to 25 μm beyond the physical beginning of the line by accurate positioning with contact marks. Several line-couples with different contact geometries (2.5 μm gold) were measured on GaAs (a thru (250 μm) and line (3200μm)) (ε_r=12.95). The contact geometries of the measured lines are given in Table 1.

The extracted error-box parameters using the Y_pZ_s-method are given in Table 1. These parameters will be compared with the simulated ones in section III.C.

Table 1: Contact geometries of the measured GaAs CPW lines together with the extracted error-box parameters (Y_pZ_s-method).

	line 1	line 2	line 3	line 4	ISS
W_{line}	80 μm	60 μm	30 μm	17 μm	50 μm
W_{slot}	10 μm	20 μm	22.5 μm	40 μm	25 μm
C_g	5.9 fF	4 fF	2.5 fF	1 fF	0.1 fF
L_s	1 pH	1 pH	1.4 pH	2 pH	0.4 pH

B. 3-D Simulation Set-up

The accuracy of the models, described in the section II, may be verified theoretically by simulating the probe-to-line interaction using a 3-D simulator (Ansoft HFSS has been used in this work). The simulated geometry is shown schematically in Figure 4. We have assumed a probe with a stripwidth of 50 μm and a probe pitch of 100 μm (S_{probe}=25 μm). After the simulation, the reference plane at the right hand side was shifted towards the probe-tip.

First, the contact to an Alumina CPW line (ISS in Table 1) is simulated (width=50μm, slot=25μm), then various contact geometries on GaAs are simulated. The Alumina-pad simulation is subsequently subtracted from these simulations to obtain the errorbox representing the differences between the off-wafer calibration and the measured line on a different substrate with a different contact geometry. Naturally, the method described above can be easily applied to a variety of substrates and contact geometries.

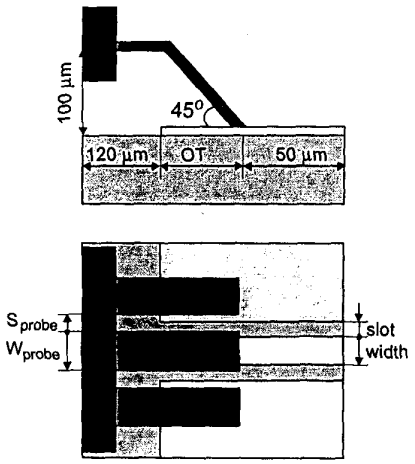

Figure 4: Geometry used to simulate the probe to contact-pad interaction (OT = overtravel).

C. 3-D Simulations: Extracted Error-box Parameters

The contact to various GaAs CPW lines (Table 2) has been simulated. The resulting parasitic capacitance to ground and series inductance, extracted from the simulations using the Y_pZ_s-method, are also given.

Table 2: Geometries of the simulated GaAs CPW lines and the resulting parasitic capacitance to ground and series inductance extracted from the simulations using the Y_pZ_s-model.

	#1	#2	#3	#4	#5	#6
W_{line} (µm)	50	80	80	60	30	17
S_{line} (µm)	25	10	10	20	22.5	40
overtravel (µm)	25	25	40	25	25	25
C_g (fF)	2.6	7.4	11.8	4.1	1.8	0.2
L_S (pH)	0.002	-0.9	-1	-0.3	-0.25	1

When comparing these results with Table 1, one may observe a very good agreement between the measured and simulated parasitic capacitances and inductances: the difference between the measured and simulated parasitic capacitance remains below 1 fF while the difference between the measured and simulated parasitic inductance remains below 2 pH (simulations have been performed up to 51 GHz, measurements up to 50 GHz). This clearly shows that 3-D simulations may be used to determine the parasitics at the probe-tip. The simulated parasitics showed to be frequency-independant as was also found from the measurements ([1, 5]).

D. 3-D Simulations: Accuracy of the Methods

The worst case error on S_{11} (expressed as $\left|S_{11}^{effective} - S_{11}^{measured}\right|$) as a function of frequency for configuration #3 and #4 (Table 2) is given in Figure 5. It can be clearly seen that compensation is necessary as the induced error may be as large as 0.35 @ 51 GHz. After compensation (Y_pZ_s-method has been used), the worst case error was reduced below 0.01. In the calculation of the error, passive structures have been assumed.

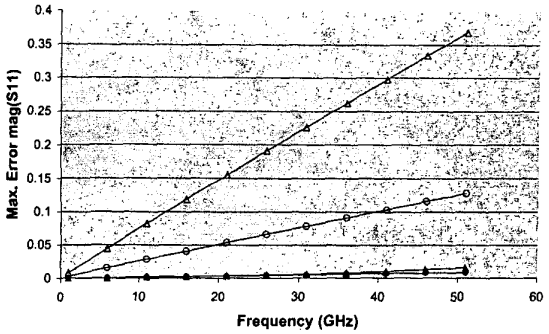

Figure 5: Worst case error on S_{11} (expressed as $\left|S_{11}^{measured} - S_{11}\right|$) for configuration #3 (Δ: uncompensated, ▲: Y_pZ_s-compensated) and #4 (o: uncompensated, •: Y_pZ_s-compensated). Passive structures have been assumed.

In Table 3, we have given the extracted errorbox parameters using the different methods for configuration #4 in Table 2. We have also given the calculated worst case error on S_{11} before and after compensation. From this, we can conclude that all methods that take the presence of a parasitic capacitance at the probe-tip into account, are capable to accurately remove the effect of the probe-tip parasitics.

Table 3: Simulated error-box parameters and worst case error for configuration #4 in Table 2.

method	parameters	max error S_{11} @ 51 GHz
uncompensated		0.128
Y_pZ_s	C_g= 4.1 fF, L_S= -0.3 pH	< 0.009
Y_pTL	C_g= 4.2 fF, d= -1 µm	< 0.009
Y-matrix	C_g= 2.1 fF, L_S= -0.3 pH	< 0.009
Z-matrix	C_g= 4.1 fF, L_S= -0.15 pH	< 0.009
Y_p	C_g= 4 fF	< 0.009
TL	d= -10 µm	0.058

E. Effect on Extracted Characteristic Impedances

3-D simulations also allow to verify the accuracy of the methods for obtaining the characteristic impedance of the lines as it is possible to compare the effective Z_c of the line with the one extracted from the embedded lines.

In Figure 6, the simulated and extracted Z_c for config. #5 (Table 2) are shown. It can be noted that the TL-method is not able to accurately obtain the effective Z_c of the line. It may be expected that this effect will be more pronounced when the capacitance to ground increases,

such as is e.g. the case on low-resistivity substrates. All other methods accurately obtain the effective Z_c of the line.

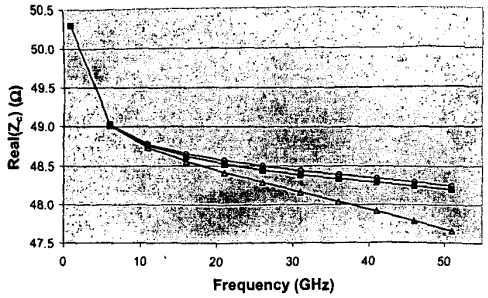

Figure 6: Extracted Z_c for configuration #5 (Table 2): (-o-) simulated Z_c using HFSS, (-+-) Y_pZ_s-method, (-x-) Y_pTL-method, (-Δ-) TL-method, (-□-) Y_p-method. The accuracy of the Y- and Z-matrix method are comparable to the Y_pTL-method.

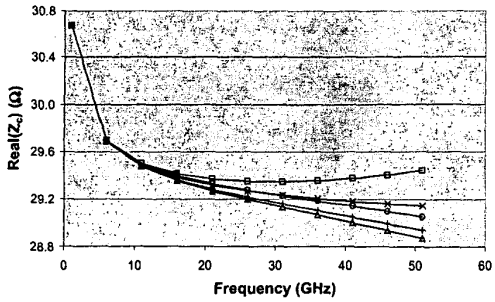

Figure 7: Extracted Z_c for configuration #3: (-o-) simulated Z_c (HFSS), (-+-) Y_pZ_s-method, (-x-) Y_pTL-method, (-Δ-) TL-method, (-□-) Y_p-method. The accuracy of the Y- and Z-matrix methods is comparable to the Y_pTL-method.

3-D simulations also make it possible to investigate the effect of an unknown probe-tip location on the extracted Z_c. In Figure 7, we have given the extracted Z_c, using the different models, for configuration #3 (Table 2): the assumed overtravel is 60 μm while the actual overtravel in the 3-D simulation is only 25 μm (probe-position error of 35 μm). It can be seen that the Y_p-method starts to deviate from the target value as it cannot account for a shift in reference plane location. It should be mentioned that the Y_pTL-method is best suited to account for a probe-position error (independent result), followed by the Y- and Z-matrix method and the Y_pZ_s-method.

F. Choice of Error-box model

The Y_pTL-method is best suited for cases where a large uncertainty in the reference plane location exists. The Y_pZ_s-method can only account for relatively small probe positioning errors, however, the method is highly suited to detect the presence of a parasitic contact resistance. The Y- and Z-matrix method perform well for practical probe position errors, however, it may be expected that the performance will deteriorate when a large shunt capacitance at the probe tip is combined with a large reference plane error. An additional advantage of the Y_pTL-model is that it can give accurate information on the reference plane location/probe tip position. The Y_p-method performs well as long as the reference plane is accurately known. Naturally, the choice of the optimal model depends on the actual uncertainties during the measurements.

In general, models using 4 parameters are preferred to the Y_p- or TL-model as they provide a higher accuracy while an equal amount of measurements is required to implement them.

CONCLUSIONS

In this paper, the accuracy of several techniques to compensate for probe-tip discontinuities has been evaluated. This has been done based on 3-D simulations. A good agreement between the measured and simulated contact parasitics has been demonstrated which shows that 3-D simulations may be used to determine the probe-tip discontinuities.

In general, we conclude that models using 4 parameters are preferred to the Y_p- or TL-model as they provide a higher accuracy while an equal amount of measurements is required to implement them.

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